SCHEME OF EXAMINATION FOR B.TECH DEGREE COURSE

Seventh Semester Examination

(Electrical & Electronics Engineering)

S No.	Course No.	Subject	Teaching Schedule				Examination Schedule				Duration of Exam (Hours)
			L	T	P/ D	Total	Theory	Sessional	Practical Viva	Total Marks	
1	----------	Departmental Elective- I	3	1	-	4	100	50	-	150	3
2	----------	Departmental Elective- II	3	1	-	4	100	50	-	150	3
3	EEcT-421E	Computer Organization & Architecture	4	1	-	5	100	50	-	150	3
4	EEcT-423E	Generation & Control of Power	3	1	-	4	100	50	-	150	3
5	EEcT-425E	Microwave & Radar Engg.	3	1	-	4	100	50	-	150	3
6	EEcT-427E	Advance Programming	4	1	-	5	100	50	-	150	3
7	EEcT-423E	Advance Programming Lab	-	-	3	3	-	25	25	50	3
7	EEcT-425E	Digital Signal Processing Lab	-	-	2	2	-	25	25	50	3
8	EEcT-427E	Minor Project	--	-	3	3	-	50	50	100	3
9	EEcT-431E	Practical Training Report	-	-	-	-	-	75	-	75	-
		Total	20	6	9	35	600	475	100	1175	

DEPARTMENTAL ELECTIVES- I

1. EEct-441E Computer aided Analysis & Design
2. EEct-443E HVDC Transmission
3. EEct-445E Power System Dynamic & Control
4. EEct-447E Power system planning

DEPATMENTAL ELECTIVES- II

1. EEct-449E Antenna & Wave Propagation
2. EEct-451E Advanced Microprocessors & interfacing
3. EEct-453E Data Communication & Networking
4. EEct-455E Operating System

B.TECH VIIth SEMESTER

COMPUTER ORGANIZATION AND ARCHITECTURE

(EEcT-401-E)

L T Total
4 1 5

Theory : 100 mks
Sessional: 50 mks
Duration: 3 Hrs

UNIT I

Evolution of computers: Generation of computer system, different types of computers, characteristics of Von Neumann architecture, Limitation of computer systems, Parallel computer structures.

Instruction formats, addressing modes and instruction types: Principles of linear pipelining, Classifications of pipeline processor, Interleaved memory organizations, Instructions and arithmetic pipelines, Design examples, vector processing requirements, characteristics of vector processing.

UNIT II

Multiprocessor: Architecture, Functional structure, Loosely coupled multiprocessors, Tightly coupled multi processor, Processor characteristics for multiprocessing, Inter-connection networks, Time shared, crossbar switch and multiport memories and multistage networks for multiprocessors, classification of multiprocessor operating system.

UNIT III

AL Unit: Construction, Integer representation, Binary half adder, full adder, Parallel Binary adder, Addition and subtraction in a parallel arithmetic element, Full adder design, BCD adder, Positive and negative BCD number, Shift operations, Basic operations, Logic operations, Multiplexer, High Speed arithmetic.

Control Unit: Construction of an instruction work, Instruction cycle and execution cycle, organization of control registers, Instruction formats, Controlling arithmetic operations, Typical Sequence of operations, Instruction set, Register transfer language, Microprogramming- Micro instruction format, Simple microprogram, Microprogramming applications.

UNIT IV

Memory: Basic concepts, memory device characteristics, semiconductor memories, static and dynamic memories. Random access and serial access memories. Memory hierarchies-cache, virtual, interleaved and associative memories.

I/O Devices: Input media, Keyboards, Mouse, Pointing Devices, character recognition (MICR & OCR), Output devices, CRT, Flat panel display, Printers, Tele printer (TTY).

NOTE: The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

References:

1. Hay, " Computer Architecture And Organizations" TMH
2. Stalling , "Computer Organization" PHI
3. Tannanbaum, "Structured Computer Organization" TMH

B.TECH VIIth SEMESTER

GENERATION & CONTROL OF POWER

(EEcT-403-E)

L T P/ D Total
3 1 - 4

Theory : 100 mks
Sessional: 50 mks
Duration: 3 Hrs

UNIT I

Load Fore-casting: Load curves, load factor, maximum demand factor, diversity factor, different types of loads, fore-casting of loads.

Power plant Economics and Selection: Choice in type of generation, choice of size of generator units and number of units, cost of electrical energy, depreciation of plant, effect of load factor on cost of electrical energy.

UNIT II

Thermal Power Plants: Choice of site, main parts and working of plants & their layout, characteristics of turbo-generators.

Hydro-Electric Plants : Choice of site, types of hydro-electric plants, capacity calculations for hydro power main parts and working of plants and their layout, characteristics of hydro- electric generators.

UNIT III

Nuclear Power Plants: Choice of site, classifications of plants main parts and working of plants and their layout.

Diesel Power Plants: Choice of site, diesel plant equipment, working and layout of the plant.

UNIT IV

Combined working of Power Plants: Advantages of combined working of different power plants, Basic load stations and Peak load stations, Economic load of thermal power plants.

Power Station Equipment and Control: Exciters, purpose & requirements of good exciters, self-excited exciter, Rotating main & pilot exciters, Brushless exciters. Voltage Regulators- purpose & requirements of good voltage Regulator, Direct acting Rheostatic type voltage regulator, static voltage regulator.

1. Speed Governing Systems: Purpose of speed governing system, Hydraulic type speed governing system for steam turbines & hydro turbines.

2. Voltage Control- Voltage control by Reactive Power Control, Voltage control by tap-changing transformers combined use of tap-changing transformer and reactive power injection, use of induction regulators.

NOTE :. The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

References:

1. Deshpande, M V : Elements of Electrical Power Station Design, wheeler publishing Co.(P) Ltd. Allhabad,1979.

2 . Gupta, B. R. : Generation of Electrical Energy, Eurrasia Publishing House, (Pvt) Ltd. New Delhi, 1983
3. Gupta, P.V. : A Course in Electrical Power, Dhanpat Rai and Sons, Delhi-6
4. Vadhera, S.S : Power Sytem Analysis and Stability, Khanna Publishers, Delhi-6, 1981.

B.TECH VIIth SEMESTER

MICROWAVE & RADAR ENGG.

(EEcT-405-E)

L T P/D Total
3 1 - 4

Theory : 100 Marks
Sessional: 50 Marks
Duration : 3 Hrs

UNIT I

Introduction to microwaves and tubes,Microwave Devices: Advantage of Microwaves, limitation of conventional tubes, Light house tube, Multicavity & Reflex klystron, Magnetron

UNIT II

Tunnel diode, Gunn diode, Parametric amplifier, masers, TWT, IMPATT, TRAPTT, Microwave solid state devices.

UNIT III

Microwave Circuits: Scattering matrix, impedance transformation & Matching, passive Microwave devices (E-plane &H-plane Tee, Magic Tee, Circulator, Attenuator, isolators, directional coupler, TE, TM & TEM modes in Rectangular wave guides, resonators, phase shifter).

UNIT IV

Radar Engg. : Introduction, Radar range equation, parameters affecting the range, Doppler effect, CW and pulse Doppler Radar, MTI delay lines and canceller, range gate pulse, MTI & Doppler radar, non coherent MTI. Noise and clutter, Radar displays, Radar signal processing, applications of radar, radio aids to navigation.

NOTE: The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

References:

1. Liao S.Y. : Microwave Circuit & Devices, PHI.
2. Skolonik M. K. : Introduction to Radar system, McGraw Hill.
3. Siegman A.E. : An introduction to lasers & Masers, McGraw Hill.
4. M. Kulkarni : Microwave & Radar Engineering, Umesh Publication.
5. Gautam A. K. : Microwave Engineering , S.K. Kataria & Sons.

B.TECH VIIth SEMESTER

ADVANCE PROGRAMMING (EEcT-407-E)

L T P/D Total	Theory : 100Marks
4 1 - 5	Sessional:50 Marks
	Duration : 3 Hrs.

UNIT I

Review of elementary data structures- arrays, stacks, queues, link list with respect to storage representation and access methods.

UNIT II

Searching methods: Sequential, binary, Indexes searches.

UNIT III

Sorting: internal and external sorting, Methods: bubble, insertion, selection, merge, heap, radix and quick sort. Comparison with respect to their efficiency.

UNIT IV

C++ Programming Language:- Concept of object oriented programming, Abstract Data type C classes , Data encapsulation , inheritance, polymorphism , virtual function templates implementation using C++.

NOTE: The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Reference:

1. Trembley and Sorenson, " An Introduction of data structures with application" McGraw Hill.
2. Goodman, S.E., and Hetedniemi, S.T, " Introduction to the design and Analysis" , McGraw Hill.
3. Herbert Schildt, " C++ Computer reference", TMH.
4. Herowitz E and Sahni S. " Fundamentals of Data Structures".

B.TECH VIIth SEMESTER

ADVANCE PROGRAMMING LAB (EEcT-423-E)

L T P/D Total	Sessional : 25Marks
- - 3 3	Practical : 25 Marks
	Total : 50 Marks
	Duration : 3 Hrs.

LIST OF PROGRAMS:-

1. Write a program to perform following operations on linked list.
   - i) Insertion of a node
   - ii) Deletion of node.
2. WAP to implement stack.
3. WAP to implement queues.
4. WAP to sort a list using following.
   - i) Insertion sort
   - ii) Quick sort
   - iii) Bubble sort
   - iv) Merge sort
   - v) Selection Sort
   - vi) Radix sort
5. WAP to find roots of quadratic equation using polymorphism.
6. WAP to find addition & multiplication of two matrices using classes.
7. WAP which shows the use of inheritance.
8. WAP to implement the concept of copy constructor & destructor.

NOTE : At least 9 experiments are to be performed with 8 from above list, remaining may either be performed or designed & set by concerned institution as per the scope.

B.TECH VIIth SEMESTER

DIGITAL SIGNAL PROCESSING LAB

EEcT-425-E

L T P Total	Sessional - 25 Marks
0 0 2 2	Practical - 25 Marks
	Total - 50Marks
	Duration - 3 Hrs

Perform the Experiments using MATLAB:-

1. To develop a program for computing Z- transform in factored form, Plot its poles and zeros , and then determine its ROCs.
2. To develop a program for computing Inverse Z-transform of a rational transfer function.
3. To develop a program for linear convolution and circular convolution .
4. To develop a Program for computing discrete fourier transform .
5. To develop a Program for computing the convolution by overlap-add method and overlap save-method.
6. To develop Program for realization of IIR Digital filters (Direct, Cascade, Parallel).
7. To develop a program for sampling theorem .
8. To design FIR filters using windows technique.
9. To design analog filter (Low pass, High pass).
10. To design analog filter (Band pass, Band stop)
11. To design IIR filters using (Impulse Invariant method).
12. To design IIR filters using (bilinear transformation).