

Roll No. ....

Total Pages : 03

**BT-4/M-20**

**34013**

**DIGITAL ELECTRONICS**

**EEcT-202E**

**Option I**

Time : Three Hours]

[Maximum Marks : 100

**Note :** Attempt *Five* questions in all, selecting at least *one* question from each Unit.

**Unit I**

1. (a) Describe De Morgan's theorems and simplify the given Boolean expression : **5**

$$Y(A, B, C, D) = \overline{(\overline{A} + C)} \cdot (\overline{B + \overline{D}})$$

- (b) Convert the following numbers :

(i)  $(86.421)_8 = (?)_2$

(ii)  $(B45.251)_{16} = (?)_{10}$

(iii)  $(412.456)_{10} = (?)_{16}$

(iv)  $(41.785)_{16} = (?)_2$

(v)  $(682.231)_8 = (?)_{10}$  **15**

2. (a) Minimize the following expressions using K-Map and realize it using NOR gate only : **10**

$$f(A, B, C, D) = \Sigma m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$$

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- (b) Describe 1's Complement and 2's Complement method and solve the following using these methods :
- (i)  $64 - 32$
- (ii)  $-48 - 25$ . **10**

### **Unit II**

3. (a) Explain the characteristics of ECL family in detail. **10**
- (b) Explain the operation of CMOS NOR gate. **10**
4. (a) Describe operation of TTL with Totem Pole output in detail. **10**
- (b) Write a technical note on MOS logic families. **10**

### **Unit III**

5. (a) Design full subtractor using half subtractors. **10**
- (b) Describe Asynchronous Counter. **5**
- (c) Write a technical note on parity generator and checker. **5**
6. (a) Explain Multiplexer, Demultiplexer and Comparator with Schematic diagrams. **15**
- (b) Draw a neat circuit diagram of clocked J-K flip-flop using NAND gates. **5**

#### Unit IV

7. (a) Explain the basic concept of Successive approximation and counter method. **10**
- (b) Explain specification and parallel-comparator of A/D converter. **10**
8. Write short notes on any *four* of the following : **5×4**
- (a) D/A Converter
  - (b) Sample and Hold Circuit
  - (c) Schmitt Trigger
  - (d) RAM & ROM
  - (e) State Transition Diagram.