Roll No. ..... **Total Pages : 03**

BT-4/M-20 34104

DIGITAL ELECTRONICS

EE-202N

Time : Three Hours] [Maximum Marks : 75

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. (a) What are BCD code and Excess-3 code ? What are the rules for BCD and Excess 3 code additions ? Explain with suitable examples. **8**

(b) Explain the rules of 1's complement and 2's complements addition and subtraction with suitable examples. **7**

2. (a) Explain different types of Logic gates and their truth tables. **8**

(b) Describe De Morgan's theorems and simplify the given Boolean expression : **7**

$$Y(A, B, C, D) = \overline{\left(\overline{A} + C\right).\left(B + \overline{D}\right)}$$

Unit II

3. Minimize the following expressions using K-Map and realize its using NOR gate only : **15**

$f(A, B, C, D) = \Sigma m (0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$

4. Explain half subtractor and full subtractor and design full subtractor using half subtractor. **15**

Unit III

5. (a) Explain D/A and A/D converter with Schematic diagrams. **8**

(b) Describe Successive Approximation Method in detail. **7**

6. (a) Explain, how a J-K flip-flop flow is converted in to D flip flop and T flip-flop. **8**

(b) Draw a neat circuit diagram of clocked J-K flip-flop using NAND gates. Give its truth table and explain race around condition. **7**

Unit IV

7. (a) Explain the characteristics of ECL family in detail. **8**

(b) Explain the operation of CMOS NOR gate. **7**

8. Write short notes on any *three* of the following : **5×3**

(a) ROM

(b) PAL

(c) FPGA

(d) CPLDS.